**UNITED STATES PATENT APPLICATION FOR:**

# METHOD OF DECREASING THE K VALUE IN SIOC LAYER DEPOSITED BY CHEMICAL VAPOR DEPOSITION


**INVENTORS:**

**FREDERIC GAILLARD**

**LI-QUN XIA**

**TIAN-HOE LIM**

**ELLIE YIEH**

**WAI-FAN YAU**

**SHIN-PUU JENG**

**KUOWEI LIU**

**YUNG-CHENG LU**


**ATTORNEY DOCKET NUMBER: AMAT/2592.C9/DSM/LOW K/JW**

**CERTIFICATION OF MAILING UNDER 37 C.F.R. 1.10**

I hereby certify that this New Application and the documents referred to as enclosed therein are being deposited with the United States Postal Service on, 2/27, 2004 in an envelope marked as "Express Mail United States Postal Service", Mailing Label No. EV335471343US, addressed to: Commissioner for Patents, Mail Stop PATENT APPLICATION, P.O. Box 1450, Alexandria, VA 22313-1450

Keith M. Tackett
Signature

Keith M. Tackett
Name

2/27/04
Date of signature

# METHOD OF DECREASING THE K VALUE IN SIOC LAYER DEPOSITED BY CHEMICAL VAPOR DEPOSITION

## BACKGROUND OF THE DISCLOSURE

### Related Applications

[0001] This application is:

a continuation of co-pending United States Patent Application No. 10/632,179 [AMAT/2592.C6], filed on July 31, 2003, which is a continuation of United States Patent Application No. 09/679,843 [AMAT/2592.P4], filed on October 5, 2000, now issued as United States Patent No. 6,627,532, which is a continuation-in-part of United States Patent Application No. 09/465,233 [AMAT/2592.C1], filed on December 16, 1999, now issued as United States Patent No. 6,511,903, which is a continuation of United States Patent Application No. 09/021,788 [AMAT/2592], which was filed on February 11, 1998, now issued as United States Patent No. 6,054,379;

a continuation-in-part of United States Patent Application No. 09/553,461 [AMAT/2592.P3], which was filed on April 19, 2000, now issued as United States Patent No. 6,593,247;

a continuation-in-part of United States Patent Application No. 09/162,915 [AMAT/3032], which was filed on September 29, 1998, now issued as United States Patent No. 6,287,990;

a continuation-in-part of United States Patent Application No. 09/185,555 [AMAT/3032.P1], which was filed on November 4, 1998, now issued as United States Patent No. 6,303,523;

and a continuation-in-part of United States Patent Application No. 09/247,381 [AMAT/3032.P2], filed on February 10, 1999, now issued as United States Patent No. 6,348,725. Each of the related applications is incorporated by reference herein.

## Field of the Invention

[0002] The present invention relates to the fabrication of integrated circuits. More particularly, the invention relates to a process for depositing dielectric layers on a substrate and the structures formed by the dielectric layer.

## BACKGROUND OF THE INVENTION

[0003] One of the primary steps in the fabrication of modern semiconductor devices is the formation of metal and dielectric films on a substrate by chemical reaction of gases. Such deposition processes are referred to as chemical vapor deposition or CVD. Conventional thermal CVD processes supply reactive gases to the substrate surface where heat-induced chemical reactions take place to produce a desired film

[0004] Semiconductor device geometries have dramatically decreased in size since such devices were first introduced several decades ago. Since then, integrated circuits have generally followed the two year/half-size rule (often called Moore's Law), which means that the number of devices that will fit on a chip doubles every two years. Today's fabrication plants are routinely producing devices having 0.35μm and even 0.18μm feature sizes, and tomorrow's plants soon will be producing devices having even smaller geometries.

[0005] In order to further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and insulators having low k (dielectric constant < 4.0) to reduce the capacitive coupling between adjacent metal lines. One such low k material is spin-on glass, such as un-doped silicon glass (USG) or fluorine-doped silicon glass (FSG), which can be deposited as a gap fill layer in a semiconductor manufacturing process.

[0006] A liner/barrier layer is typically deposited between subsequently deposited conductive materials and the low k dielectric material to prevent diffusion of byproducts such as moisture onto the conductive materials. For example, moisture that can be generated during formation of a low k insulator readily diffuses to the surface of the conductive metal and increases the resistivity of the conductive metal surface. A barrier/liner layer formed from conventional silicon oxide or silicon nitride

materials can block the diffusion of the byproducts. Similarly, a capping layer may be deposited on a low k dielectric gap film to prevent diffusion of contaminants such as moisture. However, the barrier/liner layers and capping layers typically have dielectric constants that are significantly greater than 4.0, and the high dielectric constants result in a combined insulator that does not significantly reduce the dielectric constant.

[0007] Therefore, there remains a need for dielectric layers having low dielectric constants and adjacent liner/barrier layers that provide an overall low dielectric constant.

## SUMMARY OF THE INVENTION

[0008] The present invention generally provides a method for depositing a silicon oxycarbide layer having a low dielectric constant and depositing a silicon and carbon containing layer on the silicon oxycarbide layer. In one aspect, the invention provides a method for processing a substrate comprising depositing a dielectric layer comprising silicon, oxygen, and carbon on the substrate, wherein the dielectric layer has a carbon content of at least 1% by atomic weight and a dielectric constant of less than about 3, and depositing a silicon and carbon containing layer on the dielectric layer. The silicon and carbon containing layer can be an amorphous silicon carbide layer that may be doped with oxygen, nitrogen, or both.

[0009] Another aspect of the invention provides for a method for processing a substrate, comprising depositing a dielectric layer on the substrate by reacting an organosilane compound and an oxidizing gas, wherein the dielectric layer has a carbon content of at least 1% by atomic weight and a dielectric constant of less than about 3, and depositing a silicon carbide layer or doped silicon carbide layer on the dielectric layer at plasma conditions sufficient to reduce the dielectric constant of the dielectric layer.

[0010] In another aspect of the invention, a method is provided for processing a substrate, comprising depositing a dielectric layer on the substrate by reacting an organosilicon compound comprising three or more alkyl groups with ozone, wherein the dielectric layer has a carbon content between about 5% and about 50% by

atomic weight and a dielectric constant less than about 3, and depositing a silicon carbide layer or doped silicon carbide layer on the dielectric layer by reacting an alkylsilane compound at plasma conditions sufficient to reduce the dielectric constant of the dielectric layer to less than about 2.4.

[0011] Another aspect of the invention provides for a substrate comprising a dielectric layer comprising silicon, oxygen, and carbon, wherein the dielectric layer has a carbon content of at least 1% by atomic weight, and a silicon and carbon containing layer capping the dielectric layer. The dielectric layer preferably has a dielectric constant less than about 2.4.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0012] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0013] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0014] Fig. 1 is a a cross-sectional diagram of an exemplary CVD reactor configured for use according to embodiments described herein;

[0015] Fig. 2 is a flow chart of a process control computer program product used in conjunction with the exemplary CVD reactor of Fig. 1;

[0016] Fig. 3 is a cross sectional view showing a damascene structure comprising a silicon oxycarbide layer and a silicon carbide cap layer described herein;

[0017] Fig. 4A-4C are cross sectional views showing one embodiment of a damascene deposition sequence;

[0018] Fig. 5 is a cross sectional view showing a dual damascene structure comprising two silicon oxycarbide layers and two silicon carbide cap layers described herein;

[0019] Fig. 6A-6E are cross sectional views showing one embodiment of a dual damascene deposition sequence;

[0020] Fig. 7 is a flow chart illustrating steps undertaken in depositing a silicon oxycarbide layer and a silicon carbide cap layer in a gap filling process according to another embodiment described herein; and;

[0021] Fig. 8A-8E is a schematic diagram of the layers deposited on a substrate by the process of Fig. 7.

[0022] For a further understanding of the present invention, reference should be made to the ensuing detailed description.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0023] The present invention is described by reference to a method and apparatus for depositing a silicon oxycarbide layer having a low dielectric constant, and depositing a silicon and carbon containing layer on the silicon oxycarbide layer. Surprisingly and unexpectedly, plasma enhanced deposition of a silicon and carbon containing layer on the silicon oxycarbide layer decreases the dielectric constant of the underlying silicon oxycarbide material, apparently by removing some of the carbon without shrinking or deforming the silicon oxycarbide layer.

[0024] The silicon oxycarbide layer is deposited by reacting an organosilicon compound to form a dielectric layer comprising carbon-silicon bonds and a dielectric constant less than about 3. The silicon oxycarbide layer can be deposited as a planar layer or as a gap fill dielectric layer between conductive materials prior to deposition of the silicon and carbon containing layer. The silicon and carbon containing layer is preferably a silicon carbide cap layer which may be doped with oxygen, nitrogen, or both.

**[0025]** The silicon oxycarbide layer contains carbon in silicon-carbon bonds which contributes to low dielectric constants and barrier properties. The remaining carbon content of the deposited film is between about 1% and about 50% by atomic weight, and is preferably between about 5% and about 50% by atomic weight. The deposited films may contain C-H or C-F bonds throughout to provide hydrophobic properties to the silicon oxycarbide layer. The inclusion of carbon-silicon bonds in the silicon oxycarbide film is believed to lower the dielectric constant to about 3 or less.

**[0026]** The silicon oxycarbide layers are produced from organosilicon compounds containing carbon in organo groups that are not readily removed by oxidation at processing conditions. Suitable organo groups include alkyl, alkenyl, cyclohexenyl, and aryl groups and functional derivatives. The organosilicon compounds include, for example:

| | |
|---|---|
| methylsilane, | $CH_3$-$SiH_3$ |
| dimethylsilane, | $(CH_3)_2$-$SiH_2$ |
| trimethylsilane, | $(CH_3)_3$-SiH |
| tetramethylsilane, | $(CH_3)_4$-Si |
| dimethylsilanediol, | $(CH_3)_2$-Si-$(OH)_2$ |
| ethylsilane, | $CH_3$-$CH_2$-$SiH_3$ |
| phenylsilane, | $C_6H_5$-$SiH_3$ |
| diphenylsilane, | $(C_6H_5)_2$-$SiH_2$ |
| diphenylsilanediol, | $(C_6H_5)_2$-Si-$(OH)_3$ |
| methylphenylsilane, | $C_6H_5$-$SiH_2$-$CH_3$ |
| disilanomethane, | $SiH_3$-$CH_2$-$SiH_3$ |
| bis(methylsilano)methane, | $CH_3$-$SiH_2$-$CH_2$-$SiH_2$-$CH_3$ |
| 1,2-disilanoethane, | $SiH_3$-$CH_2$-$CH_2$-$SiH_3$ |
| 1,2-bis(methylsilano)ethane, | $CH_3$-$SiH_2$-$CH_2$-$CH_2$-$SiH_2$-$CH_3$ |
| 2,2-disilanopropane, | $SiH_3$-$C(CH_3)_2$-$SiH_3$ |
| 1,3,5-trisilano-2,4,6-trimethylene, | -(-$SiH_2CH_2$-)$_3$ - (cyclic) |
| dimethyldimethoxysilane, | $(CH_3)_2$-Si-$(OCH_3)_2$ |
| diethyldiethoxysilane, | $(CH_3CH_2)_2$-Si-$(OCH_2CH_3)_2$ |
| dimethyldiethoxysilane, | $(CH_3)_2$-Si-$(OCH_2CH_3)_2$ |

| | |
|---|---|
| diethyldimethoxysilane, | $(CH_3CH_2)_2$-Si-$(OCH_3)_2$ |
| 1,3-dimethyldisiloxane, | $CH_3$-$SiH_2$-O-$SiH_2$-$CH_3$ |
| 1,1,3,3-tetramethyldisiloxane, | $(CH_3)_2$-SiH-O-SiH-$(CH_3)_2$ |
| hexamethyldisiloxane, | $(CH_3)_3$-Si-O-Si-$(CH_3)_3$ |
| 1,3-bis(silanomethylene)disiloxane, | $(SiH_3$-$CH_2$-$SiH_2$-$)_2$-O |
| bis(1-methyldisiloxanyl)methane, | $(CH_3$-$SiH_2$-O-$SiH_2$-$)_2$-$CH_2$ |
| 2,2-bis(1-methyldisiloxanyl)propane, | $(CH_3$-$SiH_2$-O-$SiH_2$-$)_2$-$C(CH_3)_2$ |
| 1,3,5,7-tetramethylcyclotetrasiloxane, | $(-SiHCH_3$-O-$)_4$ - (cyclic) |
| octamethylcyclotetrasiloxane, | $(-Si(CH_3)_2$-O-$)_4$ - (cyclic) |
| 1,3,5,7,9-pentamethylcyclopentasiloxane, | $(-SiHCH_3$-O-$)_5$- (cyclic) |
| 1,3,5,7-tetrasilano-2,6-dioxy-4,8-dimethylene, | $(-SiH_2$-$CH_2$-$SiH_2$-O-$)_2$- (cyclic) |
| 1,3,5-trisilanetetrahydropyran, | -$SiH_2$-$CH_2$-$SiH_2$-$CH_2$-$SiH_2$-O- (cyclic) |
| 2,5-disilanetetrahydrofuran, | -$SiH_2$-$CH_2$-$CH_2$-$SiH_2$-O- (cyclic), |
| and fluorinated derivatives thereof. | |

**[0027]** In a preferred aspect of the invention, the silicon oxycarbide layer is deposited by reacting an organosilicon compound comprising three or more alkyl groups with an oxidizing gas comprising ozone. The silicon oxycarbide layer may be deposited without an oxidizer if the organosilicon compound includes oxygen. The preferred organosilicon compounds include:

| | |
|---|---|
| trimethylsilane, | $(CH_3)_3$-SiH |
| tetramethylsilane, | $(CH_3)_4$-Si |
| 1,1,3,3-tetramethyldisiloxane, | $(CH_3)_2$-SiH-O-SiH-$(CH_3)_2$ |
| hexamethyldisiloxane, | $(CH_3)_3$-Si-O-Si-$(CH_3)_3$ |
| 2,2-bis(1-methyldisiloxanyl)propane, | $(CH_3$-$SiH_2$-O-$SiH_2$-$)_2$-$C(CH_3)_2$ |
| 1,3,5,7-tetramethylcyclotetrasiloxane, | -$(-SiHCH_3$-O-$)_4$ - (cyclic) |
| octamethylcyclotetrasiloxane, | -$(-Si(CH_3)_2$-O-$)_4$ - (cyclic) |
| 1,3,5,7,9-pentamethylcyclopentasiloxane, | -$(-SiHCH_3$-O-$)_5$- (cyclic) |
| and fluorinated derivatives thereof. | |

**[0028]** The most preferred organosilicon compound is trimethylsilane which is a preferred alkylsilane for making amorphous silicon carbide layers as described in more detail below.

**[0029]** The organosilicon compounds are oxidized during deposition of the silicon oxycarbide layer, preferably by reaction with oxygen ($O_2$), ozone ($O_3$), nitrous oxide ($N_2O$), carbon monoxide (CO), carbon dioxide ($CO_2$), water ($H_2O$), or combinations thereof. When ozone is used as an oxidizing gas, an ozone generator typically converts about 15 wt.% of the oxygen in a source gas to ozone, with the remainder typically being oxygen. However, the ozone concentration may be increased or decreased based upon the amount of ozone desired and the type of ozone generating equipment used. Organosilicon compounds that contain oxygen may be disassociated to provide the oxygen.

**[0030]** The organosilane compounds are oxidized during deposition such that the carbon content of the deposited film between about 1% and about 50 % by atomic weight, preferably about 5% and about 50%. During deposition of the silicon oxycarbide layer, the substrate is maintained at a temperature between about -20°C and about 500°C, and preferably is maintained at a temperature between about 170°C and about 180°C.

**[0031]** Following deposition, the deposited dielectric material can be annealed at a temperature between about 100°C and about 400°C for between about 1 minute and about 60 minutes, preferably at about 30 minutes, to reduce the moisture content and increase the solidity and hardness of the dielectric material, if desired. The anneal is preferably performed after the deposition of the next layer which prevents shrinkage or deformation of the dielectric layer. Inert gases, such as argon and helium, may be added to the annealing atmosphere.

**[0032]** For a plasma enhanced deposition of the silicon oxycarbide layer, the organosilicon material is deposited using a power density ranging between about 0.03 W/cm$^2$ and about 3.2 W/cm$^2$, which is a RF power level of between about 10 W and about 1000 W for a 200 mm substrate. The silicon oxycarbide layer can be deposited continuously or with interruptions, such as changing chambers or providing cooling time, to improve porosity. The RF power can be provided at a high

frequency such as between 13 MHz and 14 MHz. The RF power can be provided continuously or in short duration cycles wherein the power is on at the stated levels for cycles less than about 200 Hz and the on cycles total between about 10% and about 30% of the total duty cycle.

**[0033]** In one embodiment of plasma enhanced deposition, oxygen or oxygen containing compounds are dissociated to increase reactivity and achieve desired oxidation of the deposited film. RF power is coupled to the deposition chamber to increase dissociation of the compounds. The compounds may also be dissociated in a microwave chamber prior to entering the deposition chamber.

**[0034]** Although deposition preferably occurs in a single deposition chamber, the silicon oxycarbide layer can be deposited sequentially in two or more deposition chambers, *e.g.*, to permit cooling of the film during deposition.

**[0035]** The silicon and carbon containing layer deposited on the silicon oxycarbide layer can include a silicon carbide material, an oxygen doped silicon carbide material, a nitrogen doped silicon carbide material, or combinations thereof. The silicon and carbon containing layer is preferably an amorphous hydrogenated silicon carbide. The amorphous silicon carbide layer is produced by the reaction of an alkysilane compound, or a carbon containing material and a silicon containing material, in a plasma of an inert gas. Oxygen or a nitrogen source, such as ammonia, may also be present during the reaction to form the doped silicon carbide layers.

**[0036]** Suitable alkylsilane compounds for depositing the silicon carbide layers include:

| | |
|---|---|
| methylsilane | ($CH_3SiH_3$) |
| dimethysilane | (($CH_3)_2SiH_2$), |
| trimethylsilane | (($CH_3)_3SiH$), |
| diethylsilane | (($C_2H_5)_2SiH_2$), |
| propylsilane | ($C_3H_7SiH_3$), |
| vinylmethylsilane | ($CH_2$=CH)$CH_3SiH_2$), |
| 1,1,2,2-tetramethyldisilane | ($HSi(CH_3)_2$—$Si(CH_3)_2H$), |

| | |
|---|---|
| hexamethyldisilane | $((CH_3)_3Si—Si(CH_3)_3)$, |
| 1,1,2,2,3,3-hexamethyltrisilane | $(H(CH_3)_2Si—Si(CH_3)_2—SiH(CH_3)_2)$, |
| 1,1,2,3,3-pentamethyltrisilane | $(H(CH_3)_2Si—SiH(CH_3)—SiH(CH_3)_2)$, |
| dimethyldisilanoethane | $(CH_3\text{-}SiH_2\text{-}(CH_2)_2\text{-}SiH_2\text{-}CH_3)$, |
| dimethyldisilanopropane | $(CH_3\text{-}SiH\text{-}(CH_2)_3\text{-}SiH\text{-}CH_3)$, |
| tetramethyldisilanoethane | $((CH)_2\text{-}SiH\text{-}(CH_2)_2\text{-}SiH\text{-}(CH)_2)$, |
| tetramethyldisilanopropane | $((CH_3)_2\text{-}Si\text{-}(CH_2)_3\text{-}Si\text{-}(CH_3)_2)$, |

and fluorinated carbon derivatives thereof.

**[0037]** The alkylsilane compounds are reacted in a plasma comprising a relatively inert gas, preferably a noble gas, such as helium or argon, or nitrogen ($N_2$). The deposited silicon carbide films have dielectric constants of about 6 or less, and preferably have dielectric constants of about 3 or less. Depositing the silicon carbide layers reduces the dielectric constant of the silicon oxycarbide layer to less than about 2.4.

**[0038]** A preferred silicon carbide layer is deposited in one embodiment by supplying trimethylsilane to a plasma processing chamber at a flow rate between about 10 and about 1000 standard cubic centimeters per minute (sccm). An inert gas, such as helium, argon, or combinations thereof, is also supplied to the chamber at a flow rate between about 50 sccm and about 5000 sccm. The chamber pressure is maintained between about 100 milliTorr and about 15 Torr. The substrate surface temperature is maintained between about 100°C and about 450°C during the deposition process. Alternatively, a doped silicon carbide layer can be deposited by introducing oxygen and/or a nitrogen source, or other dopant, into the processing chamber at a flow rate between about 50 sccm and about 10,000 sccm.

**[0039]** The organosilicon compound, inert gas, and optional dopant, are introduced to the processing chamber via a gas distribution plate spaced between about 200 millimeters (mm) and about 600 millimeters from the substrate on which the silicon carbide layer is being deposited upon. Power from a single 13.56 MHz RF power source is supplied to the chamber 10 to form the plasma at a power density between about 0.3 watts/cm$^2$ and about 3.2 watts/cm$^2$, or a power level between about 100 watts and about 1000 watts for a 200 mm substrate. A power

density between about 0.9 watts/cm$^2$ and about 2.3 watts/cm$^2$, or a power level between about 300 watts and about 700 watts for a 200 mm substrate, is preferably supplied to the processing chamber to generate the plasma. Additionally, the ratio of the silicon source to the dopant in the gas mixture should have a range between about 1:1 and about 1:100. The above process parameters provide a deposition rate for the silicon carbide layer in a range between about 100 Å/min and about 3000 Å/min when implemented on a 200 mm (millimeter) substrate in a deposition chamber available from Applied Materials, Inc., located in Santa Clara, California.

**[0040]** Processes for depositing silicon carbide layers with low dielectric constants are more fully described in co-pending United States Patent Application Serial No. 09/165,248, filed October 1, 1998, in co-pending United States Patent Application Serial No. 09/270,039, filed March 16, 1999, and in co-pending United States Patent Application Serial No. 09/627,667, filed July 28, 2000, which descriptions are incorporated by reference herein to the extent not inconsistent with the invention. The embodiments described herein for depositing silicon carbide layers are provided to illustrate the invention, the particular embodiment shown should not be used to limit the scope of the invention. The invention also contemplates other processes and materials used to deposit silicon carbide layers.

**[0041]** The deposition process of the present invention can be performed in a substrate processing system as described in more detail below.

**Exemplary CVD Reactor**

**[0042]** Figure 1 shows a vertical, cross-section view of a parallel plate chemical vapor deposition processing chamber 10 having a high vacuum region 15. The processing chamber 10 contains a gas distribution manifold 11 for dispersing process gases through perforated holes in the manifold to a substrate or substrate (not shown) that rests on a substrate support plate or susceptor 12 which is raised or lowered by a lift motor 14. A liquid injection system (not shown), such as typically used for liquid injection of TEOS, may also be provided for injecting a liquid organosilicon compound.

[0043] The processing chamber 10 includes heating of the process gases and substrate, such as by resistive heating coils (not shown) or external lamps (not shown). Referring to Fig. 1, susceptor 12 is mounted on a support stem 13 so that susceptor 12 (and the substrate supported on the upper surface of susceptor 12) can be controllably moved between a lower loading/off-loading position and an upper processing position which is closely adjacent to manifold 11.

[0044] When susceptor 12 and the substrate are in processing position 14, they are surrounded by an insulator 17 and process gases exhaust into a manifold 24. During processing, gases inlet to manifold 11 are uniformly distributed radially across the surface of the substrate. A vacuum pump 32 having a throttle valve controls the exhaust rate of gases from the chamber.

[0045] Before reaching manifold 11, deposition and carrier gases are input through gas lines 18 into a mixing system 19 where they are combined and then sent to manifold 11. Generally, the process gases supply line 18 for each of the process gases also includes (i) safety shut-off valves (not shown) that can be used to automatically or manually shut off the flow of process gas into the chamber, and (ii) mass flow controllers (also not shown) that measure the flow of gas through the gas supply lines. When toxic gases are used in the process, several safety shut-off valves are positioned on each gas supply line in conventional configurations.

[0046] The deposition process performed in processing chamber 10 can be either a thermal process or a plasma enhanced process. In a plasma process, a controlled plasma is typically formed adjacent to the substrate by RF energy applied to distribution manifold 11 from RF power supply 25 (with susceptor 12 grounded). Alternatively, RF power can be provided to the susceptor 12 or RF power can be provided to different components at different frequencies. RF power supply 25 can supply either single or mixed frequency RF power to enhance the decomposition of reactive species introduced into the high vacuum region 15. A mixed frequency RF power supply typically supplies power at a high RF frequency (RF1) of 13.56 MHz to the distribution manifold 11 and at a low RF frequency (RF2) of 360 KHz to the susceptor 12. The silicon oxycarbide layers of the present invention are most

preferably produced using low levels of constant high frequency RF power or pulsed levels of high frequency RF power.

**[0047]** When additional dissociation of the oxidizing gas is desired, an optional microwave chamber 28 can be used to input from between about 0 Watts and about 6000 Watts of microwave power to the oxidizing gas prior to entering the deposition chamber. Separate addition of microwave power would avoid excessive dissociation of the organosilicon compounds prior to reaction with the oxidizing gas. A gas distribution plate having separate passages for the organosilicon compound and the oxidizing gas is preferred when microwave power is added to the oxidizing gas.

**[0048]** Typically, any or all of the chamber lining, distribution manifold 11, susceptor 12, and various other reactor hardware is made out of material such as aluminum or anodized aluminum. An example of such a CVD reactor is described in U.S. Patent 5,000,113, entitled A Thermal CVD/PECVD Reactor and Use for Thermal Chemical Vapor Deposition of Silicon Dioxide and *In-situ* Multi-step Planarized Process, issued to *Wang et al.* and assigned to Applied Materials, Inc., the assignee of the present invention.

**[0049]** The lift motor 14 raises and lowers susceptor 12 between a processing position and a lower, substrate-loading position. The motor, the gas mixing system 19, and the RF power supply 25 are controlled by a system controller 34 over control lines 36. The reactor includes analog assemblies, such as mass flow controllers (MFCs) and standard or pulsed RF generators, that are controlled by the system controller 34 which executes system control software stored in a memory 38, which in the preferred embodiment is a hard disk drive. Motors and optical sensors are used to move and determine the position of movable mechanical assemblies such as the throttle valve of the vacuum pump 32 and motor for positioning the susceptor 12.

**[0050]** The system controller 34 controls all of the activities of the CVD reactor and a preferred embodiment of the controller 34 includes a hard disk drive, a floppy disk drive, and a card rack. The card rack contains a single board computer (SBC), analog and digital input/output boards, interface boards and stepper motor controller boards. The system controller conforms to the Versa Modular Europeans (VME)

standard which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data but and 24-bit address bus.

[0051] The system controller 34 operates under the control of a computer program stored on the hard disk drive 38. The computer program dictates the timing, mixture of gases, RF power levels, susceptor position, and other parameters of a particular process.

[0052] Referring to Fig. 2, the process can be implemented using a computer program product 210 that runs on, for example, the system controller 34. The computer program code can be written in any conventional computer readable programming language such as for example 68000 assembly language, C, C++, or Pascal. Suitable program code is entered into a single file, or multiple files, using a conventional text editor, and stored or embodied in a computer usable medium, such as a memory system of the computer. If the entered code text is in a high level language, the code is compiled, and the resultant compiler code is then linked with an object code of precompiled windows library routines. To execute the linked compiled object code, the system user invokes the object code, causing the computer system to load the code in memory, from which the CPU reads and executes the code to perform the tasks identified in the program.

[0053] Fig. 2 shows an illustrative block diagram of the hierarchical control structure of the computer program 210. A user enters a process set number and process chamber number into a process selector subroutine 220 in response to menus or screens displayed on the CRT monitor by using the light pen interface. The process sets are predetermined sets of process parameters necessary to carry out specified processes, and are identified by predefined set numbers. The process selector subroutine 220 the (i) selects a desired process chamber on a cluster tool such as an Centura® platform (available from Applied Materials, Inc.), and (ii) selects a desired set of process parameters needed to operate the process chamber for performing the desired process. The process parameters for performing a specific process relate to process conditions such as, for example, process gas composition and flow rates, temperature, pressure, plasma conditions such as RF

bias power levels and magnetic field power levels, cooling gas pressure, and chamber wall temperature and are provided to the user in the form of a recipe. The parameters specified by the recipe are entered utilizing the light pen/CRT monitor interface.

**[0054]** The signals for monitoring the process are provided by the analog input and digital input boards of system controller and the signals for controlling the process are output on the analog output and digital output boards of the system controller 34.

**[0055]** A process sequencer subroutine 230 comprises program code for accepting the identified process chamber and set of process parameters from the process selector subroutine 220, and for controlling operation of the various process chambers. Multiple users can enter process set numbers and process chamber numbers, or a user can enter multiple process chamber numbers, so the sequencer subroutine 230 operates to schedule the selected processes in the desired sequence. Preferably the sequencer subroutine 230 includes computer readable program code to perform the steps of (i) monitoring the operation of the process chambers to determine if the chambers are being used, (ii) determining what processes are being carried out in the chambers being used, and (iii) executing the desired process based on availability of a process chamber and type of process to be carried out. Conventional methods of monitoring the process chambers can be used, such as polling. When scheduling which process is to be executed, the sequencer subroutine 230 can be designed to take into consideration the present condition of the process chamber being used in comparison with the desired process conditions for a selected process, or the "age" of each particular user entered request, or any other relevant factor a system programmer desires to include for determining the scheduling priorities.

**[0056]** Once the sequencer subroutine 230 determines which process chamber and process set combination is going to be executed next, the sequencer subroutine 230 causes execution of the process set by passing the particular process set parameters to a chamber manager subroutine 240 which controls multiple processing tasks in a process chamber 10 according to the process set determined

by the sequencer subroutine 230. For example, the chamber manager subroutine 240 comprises program code for controlling CVD process operations in the process chamber 10. The chamber manager subroutine 240 also controls execution of various chamber component subroutines which control operation of the chamber component necessary to carry out the selected process set. Examples of chamber component subroutines are susceptor control subroutine 250, process gas control subroutine 260, pressure control subroutine 270, heater control subroutine 280, and plasma control subroutine 290. Those having ordinary skill in the art would readily recognize that other chamber control subroutines can be included depending on what processes are desired to be performed in the processing chamber 10.

**[0057]** In operation, the chamber manager subroutine 240 selectively schedules or calls the process component subroutines in accordance with the particular process set being executed. The chamber manager subroutine 240 schedules the process component subroutines similarly to how the sequencer subroutine 230 schedules which process chamber 10 and process set is to be executed next. Typically, the chamber manager subroutine 240 includes steps of monitoring the various chamber components, determining which components needs to be operated based on the process parameters for the process set to be executed, and causing execution of a chamber component subroutine responsive to the monitoring and determining steps.

**[0058]** Operation of particular chamber component subroutines will now be described with reference to Fig. 2. The susceptor control positioning subroutine 250 comprises program code for controlling chamber components that are used to load the substrate onto the susceptor 12, and optionally to lift the substrate to a desired height in the processing chamber 10 to control the spacing between the substrate and the gas distribution manifold 11. When a substrate is loaded into the processing chamber 10, the susceptor 12 is lowered to receive the substrate, and thereafter, the susceptor 12 is raised to the desired height in the chamber, to maintain the substrate at a first distance or spacing from the gas distribution manifold 11 during the CVD process. In operation, the susceptor control subroutine 250 controls movement of the susceptor 12 in response to process set parameters that are transferred from the chamber manager subroutine 240.

[0059] The process gas control subroutine 260 has program code for controlling process gas composition and flow rates. The process gas control subroutine 260 controls the open/close position of the safety shut-off valves, and also ramps up/down the mass flow controllers to obtain the desired gas flow rate. The process gas control subroutine 260 is invoked by the chamber manager subroutine 240, as are all chamber components subroutines, and receives from the chamber manager subroutine process parameters related to the desired gas flow rates. Typically, the process gas control subroutine 260 operates by opening the gas supply lines, and repeatedly (i) reading the necessary mass flow controllers, (ii) comparing the readings to the desired flow rates received from the chamber manager subroutine 240, and (iii) adjusting the flow rates of the gas supply lines as necessary. Furthermore, the process gas control subroutine 260 includes steps for monitoring the gas flow rates for unsafe rates, and activating the safety shut-off valves when an unsafe condition is detected.

[0060] In some processes, an inert gas such as helium or argon is flowed into the processing chamber 10 to stabilize the pressure in the chamber before reactive process gases are introduced into the chamber. For these processes, the process gas control subroutine 260 is programmed to include steps for flowing the inert gas into the chamber 10 for an amount of time necessary to stabilize the pressure in the chamber, and then the steps described above would be carried out. Additionally, when a process gas is to be vaporized from a liquid precursor, for example 1,3,5-trisilano-2,4,6-trimethylene (1,3,5-trisilanacyclohexane), the process gas control subroutine 260 would be written to include steps for bubbling a delivery gas such as helium through the liquid precursor in a bubbler assembly. For this type of process, the process gas control subroutine 260 regulates the flow of the delivery gas, the pressure in the bubbler, and the bubbler temperature in order to obtain the desired process gas flow rates. As discussed above, the desired process gas flow rates are transferred to the process gas control subroutine 260 as process parameters. Furthermore, the process gas control subroutine 260 includes steps for obtaining the necessary delivery gas flow rate, bubbler pressure, and bubbler temperature for the desired process gas flow rate by accessing a stored table containing the necessary values for a given process gas flow rate. Once the necessary values are obtained,

the delivery gas flow rate, bubbler pressure and bubbler temperature are monitored, compared to the necessary values and adjusted accordingly.

**[0061]** The pressure control subroutine 270 comprises program code for controlling the pressure in the processing chamber 10 by regulating the size of the opening of the throttle valve in the exhaust pump 32. The size of the opening of the throttle valve is set to control the chamber pressure to the desired level in relation to the total process gas flow, size of the process chamber, and pumping set point pressure for the exhaust pump 32. When the pressure control subroutine 270 is invoked, the desired, or target pressure level is received as a parameter from the chamber manager subroutine 240. The pressure control subroutine 270 operates to measure the pressure in the processing chamber 10 by reading one or more conventional pressure manometers connected to the chamber, compare the measure value(s) to the target pressure, obtain PID (proportional, integral, and differential) values from a stored pressure table corresponding to the target pressure, and adjust the throttle valve according to the PID values obtained from the pressure table. Alternatively, the pressure control subroutine 270 can be written to open or close the throttle valve to a particular opening size to regulate the processing chamber 10 to the desired pressure.

**[0062]** The heater control subroutine 280 comprises program code for controlling the temperature of the heat modules or radiated heat that is used to heat the susceptor 12. The heater control subroutine 280 is also invoked by the chamber manager subroutine 240 and receives a target, or set point, temperature parameter. The heater control subroutine 280 measures the temperature by measuring voltage output of a thermocouple located in a susceptor 12, compares the measured temperature to the set point temperature, and increases or decreases current applied to the heat module to obtain the set point temperature. The temperature is obtained from the measured voltage by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial. The heater control subroutine 280 gradually controls a ramp up/down of current applied to the heat module. The gradual ramp up/down increases the life and reliability of the heat module. Additionally, a built-in-fail-safe mode can be

included to detect process safety compliance, and can shut down operation of the heat module if the processing chamber 10 is not properly set up.

[0063] The plasma control subroutine 290 comprises program code for setting the RF bias voltage power level applied to the process electrodes in the processing chamber 10, and optionally, to set the level of the magnetic field generated in the reactor. Similar to the previously described chamber component subroutines, the plasma control subroutine 290 is invoked by the chamber manager subroutine 240.

[0064] The above CVD system description is mainly for illustrative purposes, and other CVD equipment such as electrode cyclotron resonance (ECR) plasma CVD devices, induction-coupled RF high density plasma CVD devices, or the like may be employed. Additionally, variations of the above described system such as variations in susceptor design, heater design, location of RF power connections and others are possible. For example, the substrate could be supported and heated by a resistively heated susceptor. The pretreatment and method for forming a pretreated layer of the present invention is not limited to any specific apparatus or to any specific plasma excitation method.

**Deposition of Silicon Oxycarbide Layer and Silicon Carbide Materials.**

[0065] A damascene structure which includes a silicon oxycarbide layer and a silicon carbide layer or doped silicon carbide layer deposited thereon is shown in Fig. 3. Conductive features 310 are disposed in substrate 300. Silicon oxycarbide is deposited as a dielectric layer 314 on a dielectric liner or barrier layer 312 of silicon carbide as described herein. The liner or barrier layer may alternatively comprise other dielectric liner and barrier materials such as silicon nitride. Silicon carbide is deposited as described herein as a cap layer 316 on the dielectric layer 314. The cap layer 316 may perform as an etch stop during further substrate processing or as a liner layer. The cap layer 316, dielectric layer 314, and dielectric liner or barrier layer 312 are pattern etched to define the openings of interconnects 317 such as lines that expose the underlying conducive features 310. A conductive liner/barrier layer 318 is deposited within the interconnects 317, and a conductive material 320 is deposited thereon to fill the interconnects 317. The substrate is typically planarized as shown after deposition.

[0066] A preferred damascene structure fabricated in accordance with the invention includes a silicon oxycarbide layer and a silicon carbide layer as shown in Fig. 3, and the method of making the structure is sequentially depicted schematically in Figs. 4A-4C, which are cross sectional views of a substrate having the steps of the invention formed thereon.

[0067] As shown in Fig. 4A, a dielectric layer 314 of a silicon oxycarbide material formed from one or more organosilicon compounds using the deposition processes described herein is deposited on the liner or barrier layer 312 to a thickness between about 5,000Å to about 10,000Å, depending on the size of the structure to be fabricated. The dielectric layer 314 may be deposited in a plasma enhanced deposition process, but is preferably deposited in a plasma-free deposition process by reacting trimethylsilane with oxygen comprising about 15 wt% ozone.

[0068] The liner or barrier layer 312 may be a silicon carbide layer from the PECVD of an alkylsilane compound using a plasma of a inert gas. The silicon carbide layer which may be doped with oxygen or nitrogen. The liner/barrier layer 312 may alternatively comprise another material, such as silicon nitride, which minimizes oxidation and/or diffusion of conductive materials, such as copper, which may comprise conductive features 310 previously formed in the substrate 300.

[0069] The cap layer 316, which includes a silicon carbide layer or doped silicon carbide layer described herein, is then deposited on the dielectric layer 314 by reaction of the trimethylsilane to a thickness of about 200 to about 1000 Å using RF power in the range between about 10 and about 1000 watts for a 200 mm substrate. The silicon carbide material may be doped with oxygen or nitrogen.

[0070] As shown in Fig. 4B, the cap layer 316, the dielectric layer 314, and the liner or barrier layer 312 are then pattern etched to define the interconnects 317 and to expose the conductive feature 310 in substrate 300. Preferably, the cap layer 316, the dielectric layer 314, and the liner or barrier layer 312 are pattern etched using conventional photolithography and etch processes for silicon carbide films. Any photo resist or other material used to pattern the cap layer 316 is removed using an oxygen strip or other suitable process.

[0071] Following etching of the deposited material and removal of photo resist materials, exposed portions of the cap layer 316, the dielectric layer 314, and the liner or barrier layer 312 may be treated with a reactive pre-clean process to remove contaminants, particulate matter, residues, and oxides that may have formed on the exposed portions of the interconnects 317 and on the surface of the substrate. The reactive pre-clean process comprises exposing the substrate to a plasma, preferably comprising hydrogen and/or an inert gas, such as argon, at a power density between of 0.03 watts/$cm^2$ and about 3.2 watts/$cm^2$, or at a power level between about 10 watts and 1000 for a 200 millimeter substrate. The processing chamber is maintained at a pressure of about 20 Torr or less and at a substrate temperature of about 450°C or less during the reactive clean process.

[0072] Referring to Figure 4C, after the cap layer 316, the dielectric layer 314, and the liner or barrier layer 312 have been etched to define the interconnects 317 and the photo resist has been removed, the interconnects 317 are filled with conductive materials 320. The structure is preferably formed with a conductive material such as aluminum, copper, tungsten or combinations thereof with a conductive barrier layer to prevent diffusion. Presently, the trend is to use copper to form the smaller features due to the low resistivity of copper (1.7 Ω-cm compared to 3.1 Ω-cm for aluminum).

[0073] Preferably, the conductive barrier layer 318 is first deposited conformally in the interconnects 317 to prevent copper migration into the surrounding silicon and/or dielectric material. Barrier layers include titanium, titanium nitride, tantalum, tantalum nitride, and combinations thereof among other conventional barrier layer materials. Thereafter, copper 320 is deposited using chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof, to form the conductive structure. Once the structure has been filled with copper or other conductive material, the surface is planarized using chemical mechanical polishing to produce the finished damascene structure shown in Figure 3.

[0074] A dual damascene structure which includes two silicon oxycarbide layers and two silicon carbide cap layers or doped silicon carbide cap layers deposited thereon is shown in Fig. 5. A conductive feature 502 is disposed in substrate 500.

The first silicon oxycarbide layer is deposited as a first dielectric layer 510 on a liner or barrier layer 512, for example a silicon carbide as described herein. A first silicon carbide cap layer 514 is deposited on the first dielectric layer 510 as described herein. The silicon carbide cap layer 514 reduces the dielectric constant of the silicon oxycarbide layer and is pattern etched to define the openings of vertical interconnects such as contacts/vias. For the dual damascene application, a second dielectric layer 518 comprising the second silicon oxycarbide layer is deposited over the patterned silicon carbide cap layer 514. The second silicon carbide cap layer 519 is deposited on the second dielectric layer 518 and pattern etched to define horizontal interconnects such as lines. An etch process is performed to define the horizontal interconnects down to the first silicon carbide layer 314 which functions as an etch stop, and to define the vertical interconnects and expose the conductive feature 502 in substrate 500 prior to filling the interconnects with a conductive material 526.

**[0075]** A preferred method for making the dual damascene structure shown in Fig. 5 is sequentially depicted in Figs. 6A-6E, which are cross sectional views of a substrate having the steps of the invention formed thereon.

**[0076]** As shown in Fig. 6A, an initial first dielectric layer 510 of a silicon oxycarbide material from the organosilicon compounds and deposition processes described herein is deposited on the liner or barrier layer 512 to a thickness between about 5,000Å and about 10,000Å, depending on the size of the structure to be fabricated. The first dielectric layer 510 may be deposited in a plasma enhanced deposition process, but is preferably deposited in a plasma-free deposition process by reacting trimethylsilane with oxygen comprising about 15 wt% ozone. The liner layer 512 may be a silicon carbide layer which may be doped with oxygen or nitrogen. The liner/barrier layer 512 may alternatively comprise another material, such as silicon nitride, which minimizes oxidation and/or diffusion of conductive materials, such as copper, which may comprise conductive features 502 previously formed in the substrate 500.

**[0077]** As shown in Fig. 6B, the first cap layer 514, which includes a silicon carbide layer or doped silicon carbide layer described herein, is then deposited on

the first dielectric layer by reaction of the trimethylsilane to a thickness between about 200 and about 1000 Å using RF power in the range between about 10 and about 1000 watts for a 200 mm substrate. The first cap layer 514 is then pattern etched to define the contact/via openings 516 and to expose first dielectric layer 510 in the areas where the contacts/vias are to be formed as shown in Fig. 6C. Preferably, the first cap layer 514 is pattern etched using conventional photolithography and etch processes for silicon carbide films.

**[0078]** After the first cap layer 514 has been etched to pattern the contacts/vias 516 and the photo resist has been removed, a second dielectric layer 518 is deposited over the first cap layer 514 to a thickness between about 5,000Å and about 10,000Å as described for the first dielectric layer 510 as shown in Fig. 6D.

**[0079]** A second cap layer 519, which includes a silicon carbide layer or doped silicon carbide layer described herein, is then deposited on the second dielectric layer 518 as described for the first cap layer 514 to a thickness of about 200 to about 1000 Å. The silicon carbide material may be doped with oxygen or nitrogen. The second cap layer 519 is then patterned to define lines 520, as described for the first cap layer 514 as shown in Fig. 6E. The lines 520 and contacts/vias 516 are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (*i.e.*, the openings for the lines and contact/via) and expose the conductive feature 502 as shown in Fig. 6F. Any photo resist or other material used to pattern and etch the second cap layer 519 is removed using an oxygen strip or other suitable process.

**[0080]** Following etching of the deposited material and removal of photo resist materials, exposed portions of the second cap layer 519, the second dielectric layer 518, the first cap layer 514, the first dielectric layer 510, and the liner or barrier layer 512 may be treated with a reactive pre-clean process to remove contaminants, particulate matter, residues, and oxides that may have formed on the exposed portions of the contact/via openings 516, the line openings 520, and the conductive feature 502. The reactive pre-clean process comprises exposing the substrate to a plasma, preferably comprising hydrogen and/or an inert gas, such as argon, at a power density between of 0.03 watts/cm$^2$ and about 3.2 watts/cm$^2$, or at a power

level between about 10 watts and 1000 for a 200 millimeter substrate. The processing chamber is maintained at a pressure of about 20 Torr or less and at a substrate temperature of about 450°C or less during the reactive clean process.

**[0081]** The metallization structure is then formed with a conductive material such as aluminum, copper, tungsten or combinations thereof. Presently, the trend is to use copper to form the smaller features due to the low resistivity of copper (1.7 Ω-cm compared to 5.1 Ω-cm for aluminum). Preferably, as shown in Fig. 6G, a conductive barrier layer 524 is first deposited conformally in the metallization pattern to prevent copper migration into the surrounding silicon and/or dielectric material. Barrier layers include titanium, titanium nitride, tantalum, tantalum nitride, and combinations thereof among other conventional barrier layer materials. Thereafter, copper 526 is deposited using either chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof to form the conductive structure. Once the structure has been filled with copper or other metal, the surface is planarized using chemical mechanical polishing as shown in Fig. 5.

**[0082]** The silicon oxycarbide layer and the silicon and carbon containing materials described herein can be used in a gap filling process as shown in Fig. 7 using the CVD chamber described above and shown in Fig. 1. Referring to Fig. 7, a substrate is positioned 700 in the processing chamber 10 and a silicon carbide liner layer is deposited 705 by a CVD or plasma enhanced CVD process from the reaction of an alkylsilane compound described above, such as trimethylsilane. The deposition step 705 can include a capacitively coupled plasma or both an inductively and a capacitively coupled plasma in the process chamber 10.

**[0083]** A silicon oxycarbide gap fill layer is then deposited 710 on the liner layer by reacting an organosilicon compound such as trimethylsilane with an oxidizer such as a combination of oxygen and ozone. The gap fill layer may then be annealed in an inert atmosphere for a period of time as needed to remove moisture and solidify the deposited material. A silicon carbide cap layer is then deposited 715 on the gap fill layer using a plasma enhanced CVD process from the reaction of an alkylsilane compound described above, such as trimethylsilane, in the plasma of a relatively inert gas. The substrate is then removed 720 from the processing chamber 10.

[0084] Referring to one embodiment in Figs. 8A-8E, the three-layer gap filling process provides a PECVD lining layer 800 by reaction of an alkylsilane compound such as trimethylsilane to produce an amorphous hydrogenated silicon carbide layer as described herein. The lining layer 800 acts as an isolation layer between a subsequent organosilicon gap fill layer 802 and the underlying substrate surface 804 and metal lines 806, 808, 810 formed on the substrate surface. The gap fill layer 802 is capped by a capping layer 812 of the amorphous hydrogenated silicon carbide layer. This process is implemented and controlled using a computer program stored in the memory 38 of a computer controller 34 for a CVD processing chamber 10.

[0085] Referring to Fig. 8A, in one embodiment, the PECVD lining layer 800 is deposited in the processing chamber 10 by introducing an organosilane compound such as trimethylsilane $(CH_3)_3SiH$, and generating a plasma of an inert gas, such as helium or argon. One exemplary processing regime includes introducing trimethylsilane to a processing chamber at a flow rate between about 30 sccm and 500 sccm, introducing helium, argon, or combinations thereof into the processing chamber at a rate between about 100 sccm and about 2000 sccm, maintaining a chamber pressure between about 3 Torr and about 10 Torr, maintaining a substrate surface temperature between about 200°C and about 400°C, and supplying between about 300 watts and 700 watts to the chamber to generate the plasma of the processing gas. The gas distribution plate 11 is spaced between about 300 mm and about 600 mm from the substrate.

[0086] Referring to Fig. 8B, the gap filling layer 802 is deposited using alkylsilane compounds as described herein. Preferred process gases for the gap filling layer 802 are trimethylsilane $(CH_3)_3SiH$ and ozone, $O_3$. In one embodiment, the deposition process includes introducing trimethylsilane at a flow rate between about 50 sccm and about 500 sccm, preferably at about 175 sccm, introducing a mixture of oxygen and ozone, where ozone comprises about 15 wt.% of the mixture, at a flow rate between about 2000 sccm and about 6000 sccm, preferably at about 5000 sccm, reacting the trimethylsilane $(CH_3)_3SiH$ and $O_3$, maintaining a chamber pressure between about 50 Torr and about 500 Torr, preferably at about 100 Torr, during deposition of the gap filling layer 802. The gap filling layer 802 may be partially cured or annealed as shown in Fig. 8C to remove solvents such as water prior to

deposition of a cap layer 812 as shown in Fig. 8D. Curing is done in the processing chamber 10 by pumping under a relatively inert gas atmosphere, such as a noble gas or nitrogen, under 10 Torr at a temperature of about 400°C for about 30 minutes.

**[0087]** Referring to Fig. 8D, after deposition of the PECVD gap filling layer 802, a capping layer 812 of amorphous hydrogenated silicon carbide is deposited thereon by the plasma processes described herein. Referring to Fig. 8E, after deposition of the capping layer, if any, the gap fill layer 802 is preferably annealed in a furnace or another chamber at a temperature between about 100°C and about 450°C to remove moisture and other solvents. Of course, processing conditions will vary according to the desired characteristics of the deposited films.

**[0088]** While the foregoing is directed to preferred embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims which follow.